On Board Computer System for Microsatellite $\mu$SAT-3

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Abstract

This work will introduce the development of the On Board Computer System (OBC) for the microsatellite $\mu$SAT-3. Because of the LEO chosen orbit, expected lifetime of the mission (2 to 3 years) and cost boundary, it is designed using commercial industrial components, not radiation hardened. The OBC is composed of two computers in cold redundancy, each with a pair of lockstep Cortex-R4 core with flash memory system backup. Each one has Error Correction Codes (EEC) on Flash and RAM interfaces, Built In Self Test for CPU and On-chip RAM and loopback on peripheral IOs. The two computers are supervised by a monitor module, made with SEU immune FPGA technology. The monitor checks for clock stability, watchdog signals, voltage levels, and Error Signaling Module from the computers. In case of a failure, it attempts to restart the computer or switch to the backup one. The OBC can be reprogrammed from ground station. The procedure of reprogramming uses the active computer to re-flash the inactive one via JTAG and checks for errors during programming via BIST.

Microsatellite $\mu$SAT-3

The $\mu$SAT-3 Microsatellite is the third generation of small vehicles designed by the Argentine Air Force. The first generation ($\mu$SAT-1 - Victor) was launched in August-1996 from Russia. It stopped responding in mid-1999.

$\mu$SAT-3 is a 30 kg satellite, designed for observation of the Argentine mainland with 10 mts/pixel resolution. It is planned to deploy in a polar sun-synchronous orbit of 700 km. Orbital correction as well as deorbit maneuvers will be possible through electric propulsion by a Pulsed Plasma Thruster.

OBC Internals

The OBC System is composed by three Printed Circuit Boards. Two of them corresponding to the active and backup computers (like the one in the figure below) and the third corresponding to the monitor hardware, made with SEU immune FPGA technology. Each board contains the central processor, external memories, power supply, drivers and interfaces to interact with the subsystems. Both computers are connected to the common bus. The backup computer remains in power-off state, and its outputs in High Z state. The active computer send to the monitor the watchdog, clock and Error Signaling Module signals. This hardware is constantly checking for the state of these variables and attempts to restart or switch computers in case of failure. When the monitor receives the command for programming sequence start, it powers on the backup computer and keep its interfaces in High Z state. When programming sequence ends up, it checks the state of the computer with the new program. In case of success, it is ready for the switch computer command.

OBC Specifications

- Cortex-R4F@160Mhz RISC 32 Bits
- 1,66 DMIPS/MHz
- FPU double precision
- 3 MB Flash with ECC
- 256 KB RAM with ECC
- Power Consumption less than 2 W
- BIST integrated diagnostics, monitoring, - Voltage & Clock, redundant Watchdog - Automatic Switch to backup in case of failure
- Total or partial reconfiguration from ground
- Processor certified for Safety Critical Apps - Functional Safety. ISO26262 - SafeRTOS Certification Option - Aerospace DO178C DAL A
- EuroCard Form Factor

Conclusions

The designed OBC can be adapted to any vehicle. It has been designed with flexibility and robustness in mind. The Operative System can be upgraded to a certified version, to comply with safety standards.

All electrical interfaces have passed the required safety standards.

Remote Programming System

The program is received through an UHF link to the active OBC. After checking for errors, it stores the program in its external flash, with a HASH security code. When the active computer receives the command to program, the sequence is started by the monitor hardware. It emulates the JTAG signals and after the flashing process, the monitor checks the state of the recently programmed computer.