FPGA IMPLEMENTATION OF A NAVIC DISCIPLINED 10MHZ REFERENCE FOR SATCOM NETWORKS

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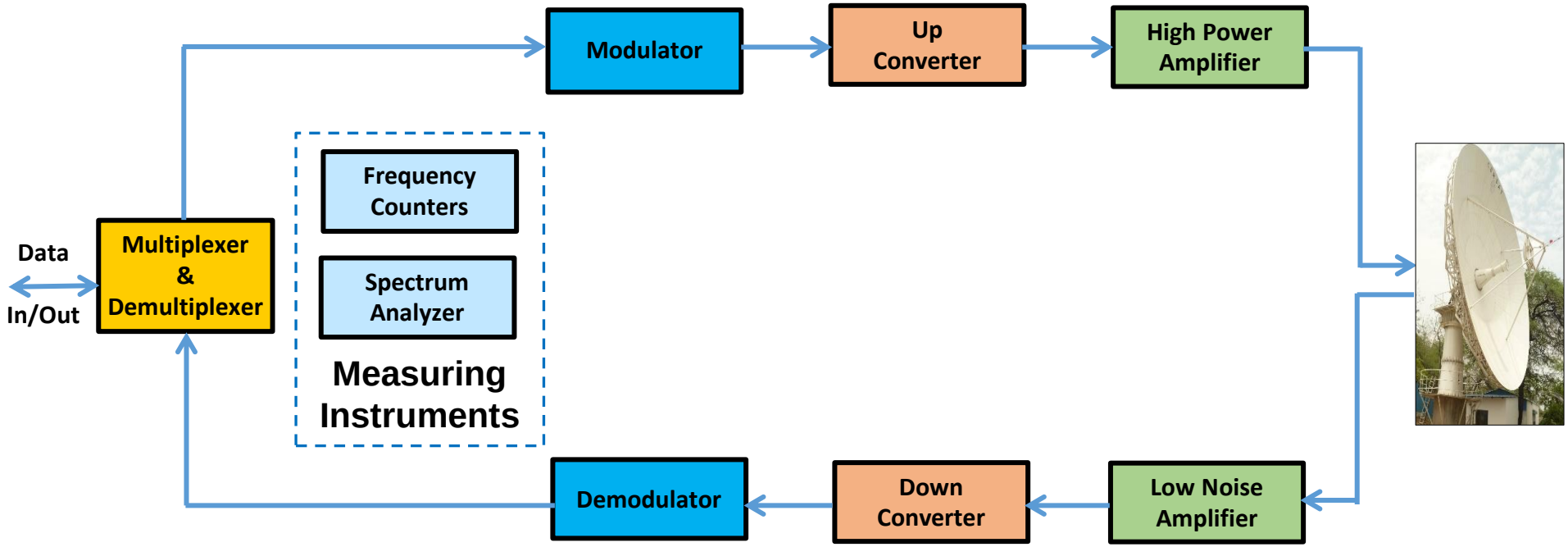
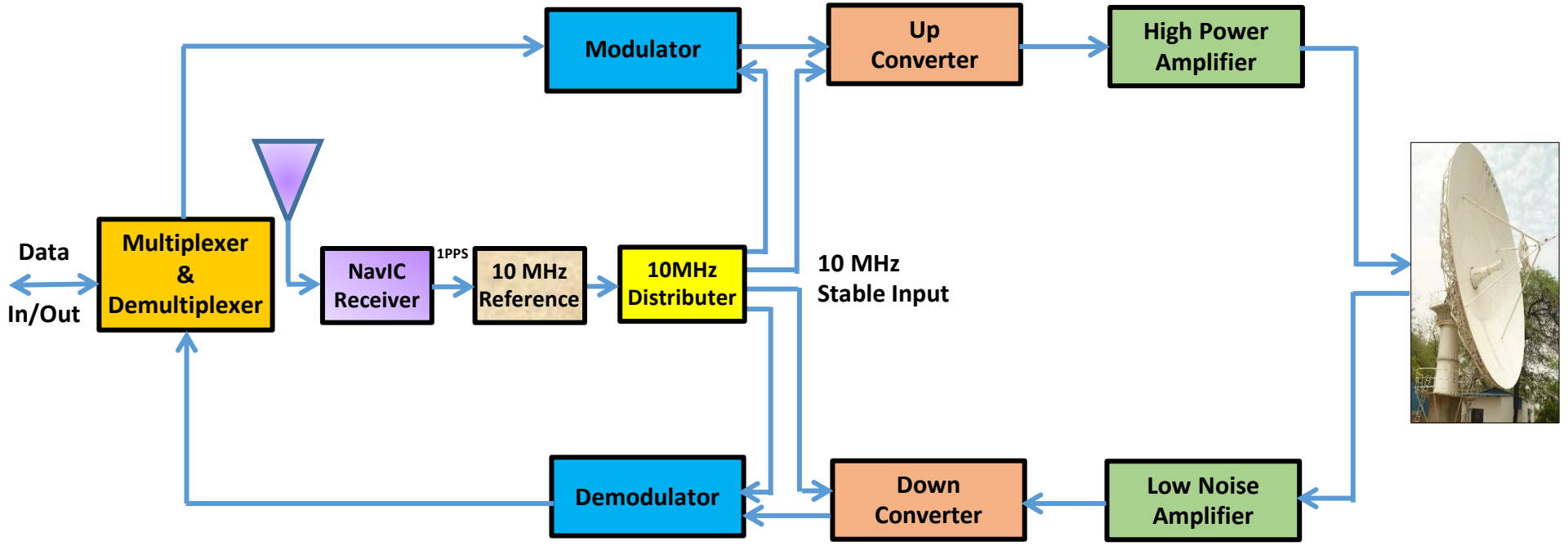
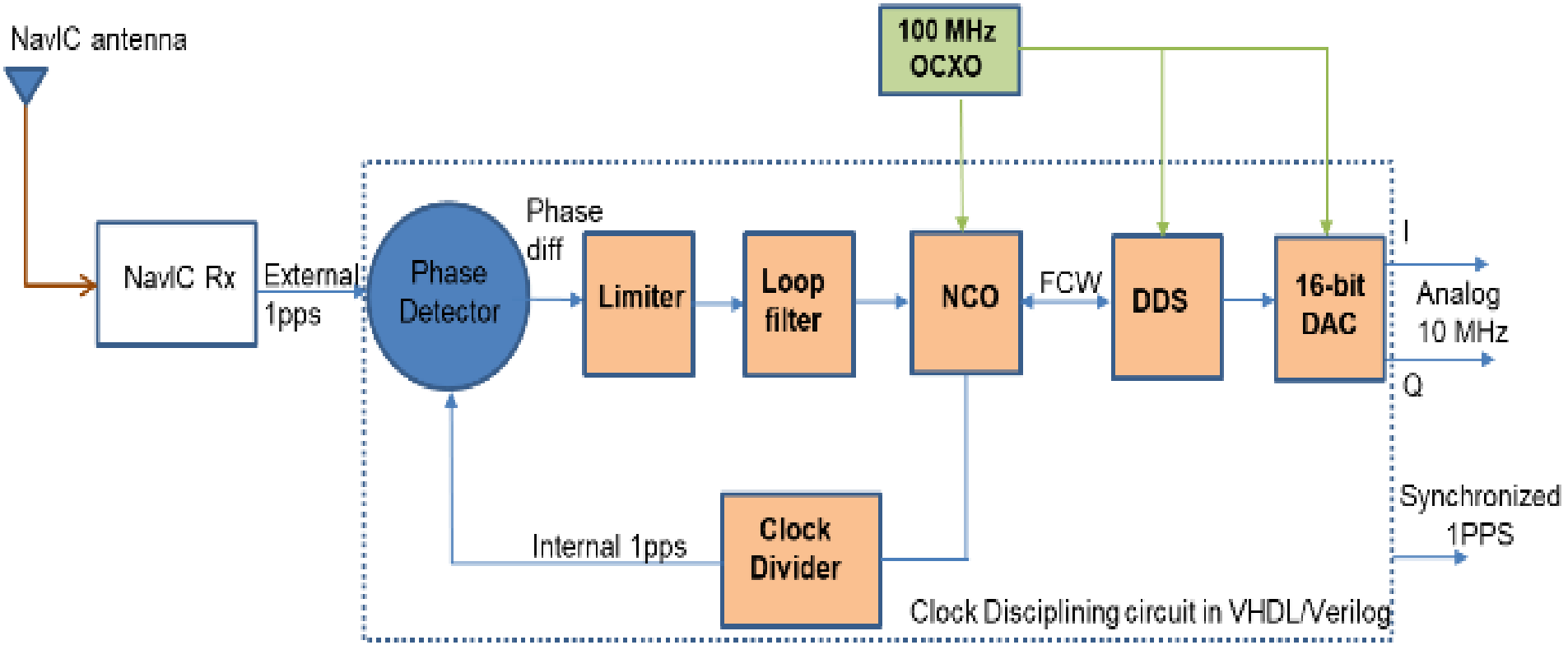
Typical Earth Station



Earth Station Synchronization Using NavIC 1 PPS Signal



Clock Disciplining Circuit



The Frequency Control Word (FCW) controls the output frequency of the DDS:

$$f_{DDS} = \frac{FCW}{2^M} f_s$$

Where, M = phase width, 32bit

f_s = Source Frequency, 100 MHz

f_{DDS} = Required frequency, 10MHz

Design Options

	Analog PLL	Discrete DAC + FPGA	DDS
Spectral Performance	High	Medium-High	Medium
Power Requirements	High	High	Low
Digital Frequency Tuning	No	Yes	Yes
Tuning Response Time	High	Low	Low
Waveform Flexibility	Low	Medium	High
Remarks	Difficult to Tune	Ability to Tune	Easy to Tune

The option of DAC interfaced with FPGA was considered

Hardware Implementation

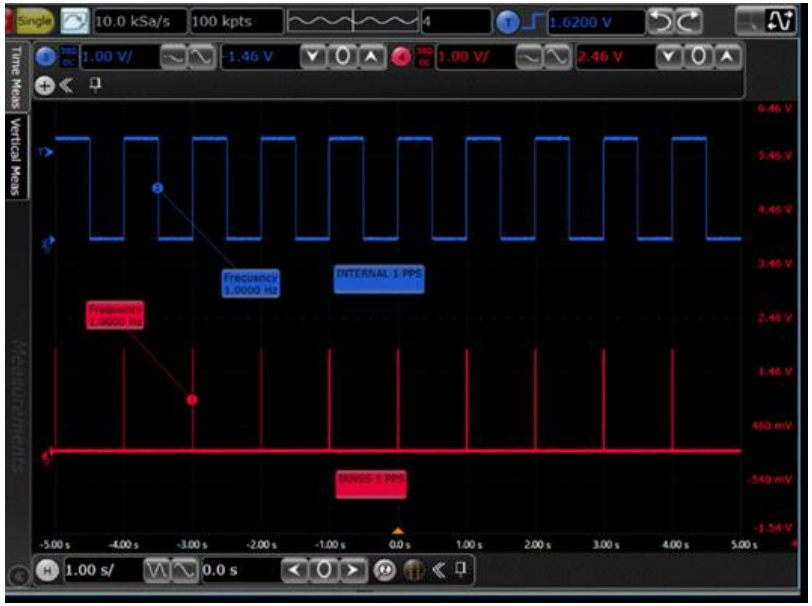
- NavIC Receiver (single band, 11 channel, SPS ASIC Rx)
- Kintex KC705 FPGA
- FMC-150 daughter card (dual channel, 16-bit D/A)
- 100MHz OCXO

Specifications of NavIC disciplined 10MHz Reference

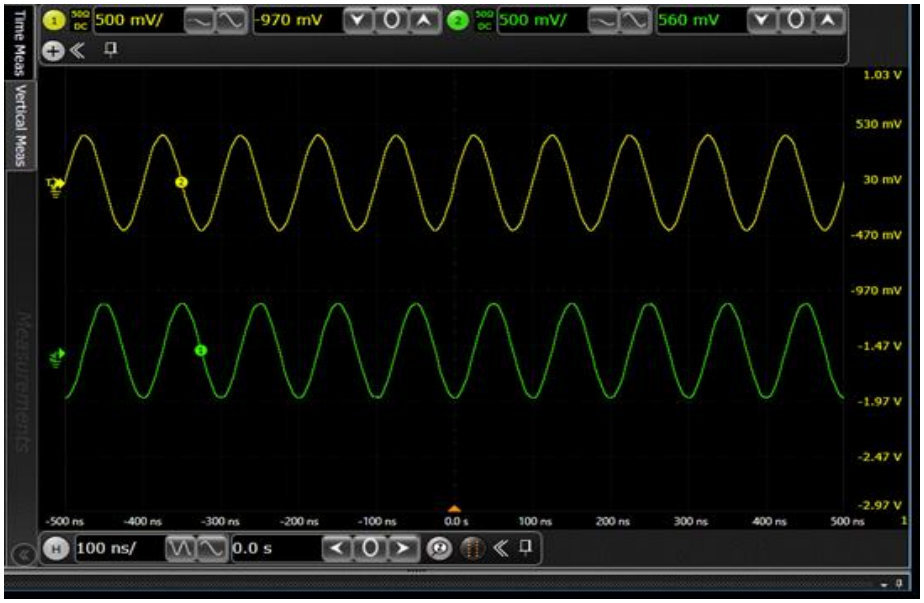
NavIC Receiver	
Frequency Band	L5
1PPS Accuracy	60 ns
TTFF	≈ 120 sec (Cold Start)
Update Rate	1 Hz
OCXO Timebase	
Oscillator Type	Oven controlled, SC-cut Crystal
Temperature stability	± 30 x 10^{-9}
Ageing	± 2 x 10^{-9} per day
Warm up time	3 min to reach within ± 0.01ppm
10 MHz Output	
Amplitude	+2.5 dBm
Harmonic Level	-60 dBc
Frequency Stability @ 25 deg C	Short term stability (1 sec): 2.1 x 10^{-10} Long term stability (10,000 sec): 1.7 x 10^{-10}
Phase Noise	
10 Hz	-98.15 dBc/Hz
100 Hz	-101.64 dBc/Hz
1 KHz	-106.74 dBc/Hz
100 KHz	-108.14 dBc/Hz

Phase Noise of 10MHz Signal vs Industry standards

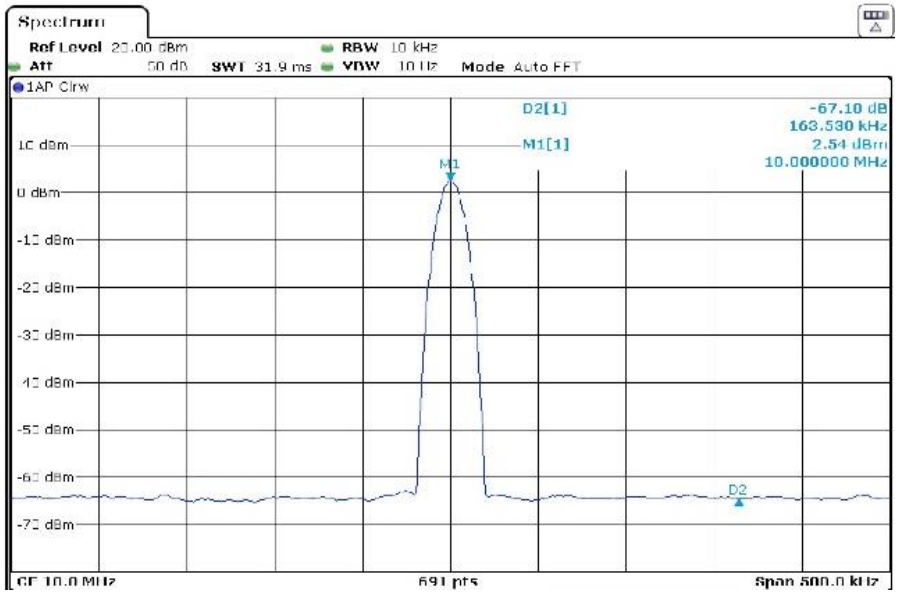
Carrier Frequency Offset	IESS 308/309 maximum allowable phase noise	Disciplined 10MHz Signal phase noise
10 Hz	-30 dBc/Hz	-98.15 dBc/Hz
100 Hz	-60 dBc/Hz	-101.64 dBc/Hz
1 KHz	-70 dBc/Hz	-106.74 dBc/Hz
100 KHz	-90 dBc/Hz	-108.14 dBc/Hz



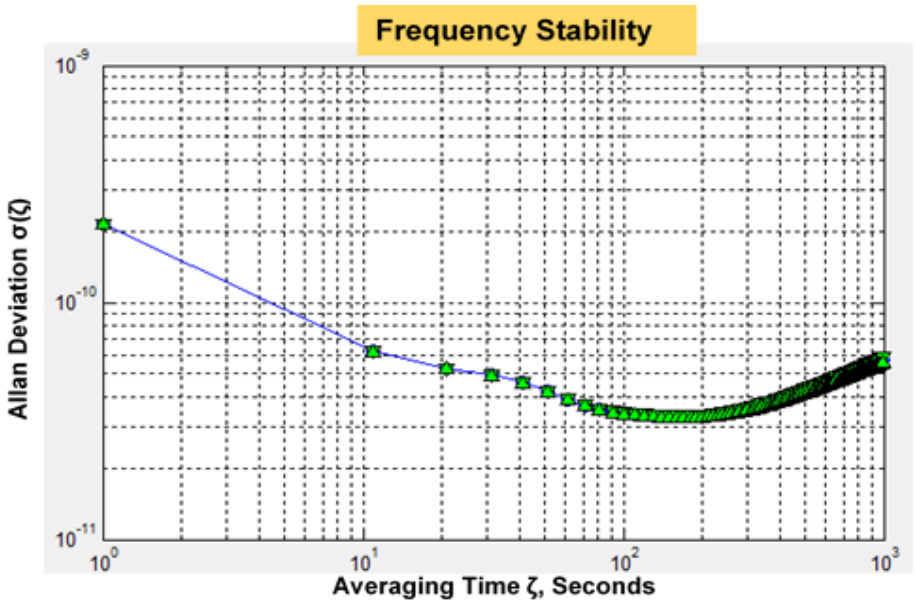
Synchronized NavIC and Internal 1PPS



10 MHz Analog Output



Spectrum of 10 MHz Analog Output



Frequency Stability Measurement

Conclusion

- NavIC 1 PPS signal was used to discipline a 100MHz OCXO to generate a reference frequency output of 10MHz.
- The disciplined output has a short term (1 sec) stability of 2.1×10^{-10} and a long term (10,000 sec) stability of 1.7×10^{-10} with phase noise better than Industry-standards.
- The power consumption of the hardware in steady state is 5.71 W.
- Developed an indigenous system guaranteed to be available to Indian users.

Thank You